

DATA SHEET

74ABT161543

74ABTH161543

16-bit latched transceiver with
dual enable and master reset (3-State)

Product specification
Supersedes data of 1995 Sep 18
IC23 Data Handbook

1998 Feb 27

16-bit latched transceiver with dual enable and master reset (3-State)

74ABT161543
74ABTH161543

FEATURES

- Two 8-bit octal transceivers with D-type latch
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- Multiple V_{CC} and GND pins minimize switching noise
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- 74ABTH161543 incorporates Bus hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Output capability: +64mA/−32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Same function as ABT16543 except for additional Master Reset control pins

DESCRIPTION

The 74ABT161543 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT161543 16-bit registered transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable (nLEAB, nLEBA) and Output Enable (nOEAB, nOEBA) inputs are provided for each register to permit independent control of data transfer in either direction. Master reset (MR) clears all registers simultaneously and sets them Low. The outputs are guaranteed to sink 64mA.

Two options are available, 74ABT161543 which does not have the Bus hold feature and 74ABTH161543 which incorporates the Bus hold feature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}$; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx	$C_L = 50\text{pF}$; $V_{CC} = 5\text{V}$	2.5 2.2	ns
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or V_{CC}	3	pF
$C_{I/O}$	I/O capacitance	$V_O = 0\text{V}$ or V_{CC} ; 3-State	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; $V_{CC} = 5.5\text{V}$	500	μA
I_{CCL}		Outputs low; $V_{CC} = 5.5\text{V}$	9	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
56-pin plastic SSOP Type III	−40°C to +85°C	BT161543DL	SOT371-1
56-pin plastic TSSOP Type II	−40°C to +85°C	BT161543DGG	SOT364-1

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	−40°C to +85°C	74ABT161543 DL	BT161543 DL	SOT371-1
56-Pin Plastic TSSOP Type II	−40°C to +85°C	74ABT161543 DGG	BT161543 DGG	SOT364-1
56-Pin Plastic SSOP Type III	−40°C to +85°C	74ABTH161543 DL	BH161543 DL	SOT371-1
56-Pin Plastic TSSOP Type II	−40°C to +85°C	74ABTH161543 DGG	BH161543 DGG	SOT364-1

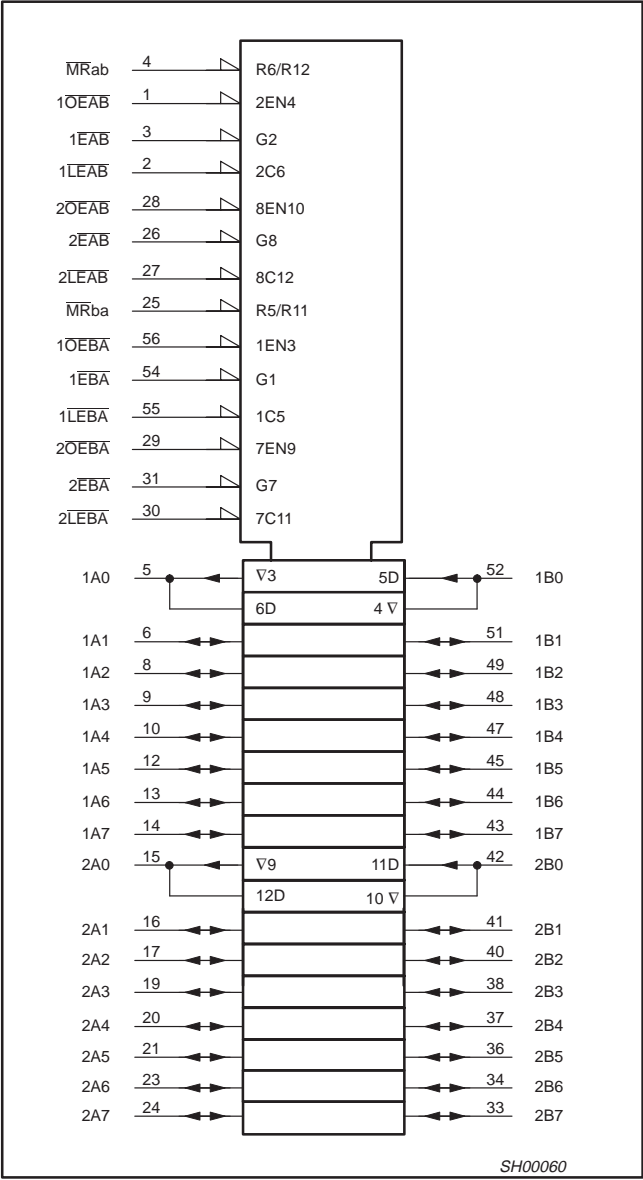
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24	1A0 – 1A7, 2A0 – 2A7	Data inputs/outputs
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33	1B0 – 1B7, 2B0 – 2B7	Data inputs/outputs
1, 56 28, 29	1OEAB, 1OEBA, 2OEAB, 2OEBA	A to B / B to A Output Enable inputs (active-Low)
3, 54 26, 31	1EAB, 1EBA, 2EAB, 2EBA	A to B / B to A Enable inputs (active-Low)
2, 55 27, 30	1LEAB, 1LEBA, 2LEAB, 2LEBA	A to B / B to A Latch Enable inputs (active-Low)
4, 25	MRab, MRba	Master reset
11, 18, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

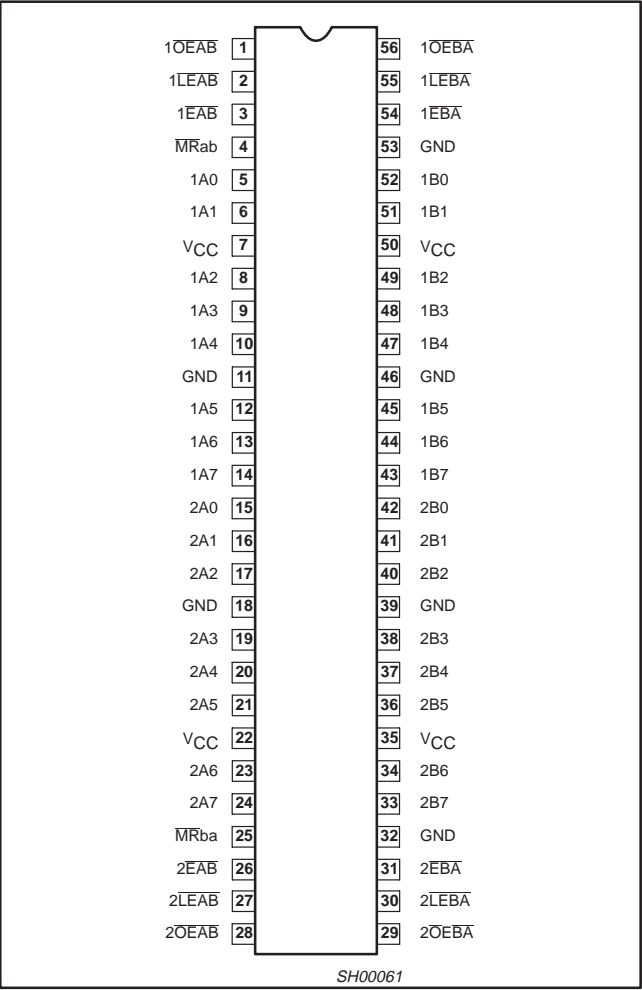
16-bit latched transceiver with dual enable
and master reset (3-State)

74ABT161543
74ABTH161543

LOGIC SYMBOL (IEEE/IEC)



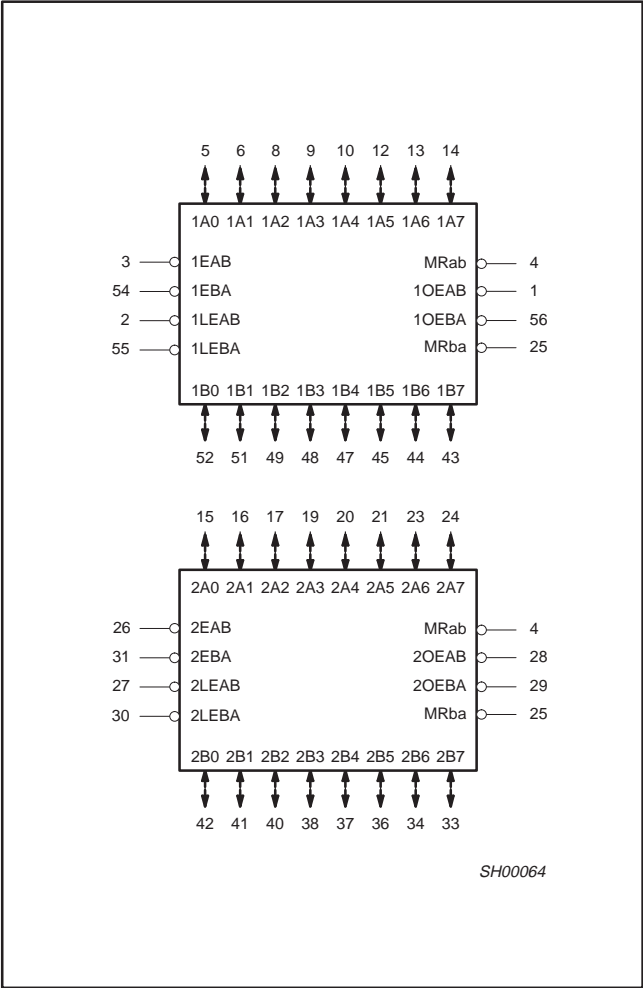
PIN CONFIGURATION



16-bit latched transceiver with dual enable
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74ABT161543
74ABTH161543

LOGIC SYMBOL



FUNCTIONAL DESCRIPTION

The 74ABT161543 contains two sets of eight D-type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B Enable (\overline{nEAB}) input and the A-to-B Latch Enable (\overline{nLEAB}) input are Low the A-to-B path is transparent.

A subsequent Low-to-High transition of the \overline{nLEAB} signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With \overline{EAB} and \overline{nOEAB} both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the \overline{nEBA} , \overline{nLEBA} , and \overline{nOEBA} inputs.

FUNCTION TABLE

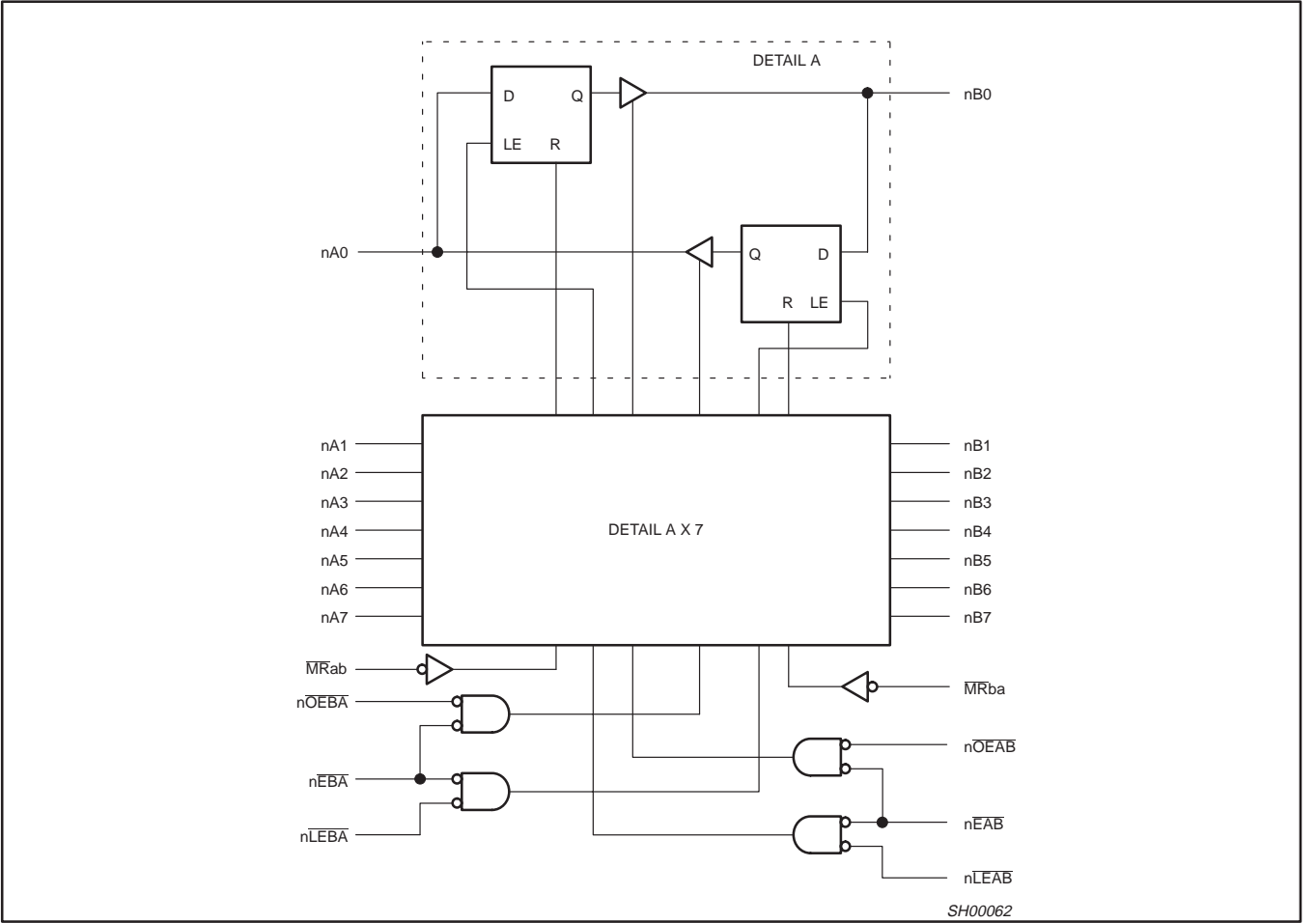
INPUTS					OUTPUTS	STATUS
\overline{nOEXX}	\overline{nMRXX}	\overline{nEXX}	\overline{nLEXX}	nAx or nBx	nBx or nAx	
L	L	L	X	X	L	Clear
H	X	X	X	X	Z	Disabled
X	X	H	X	X	Z	Disabled
L	H	\uparrow	L	h	Z	Disabled + Latch
L	H	\uparrow	L	l	Z	
L	H	L	\uparrow	h	H	Latch + Display
L	H	L	\uparrow	l	L	
L	H	L	L	H	H	Transparent
L	H	L	L	L	L	
L	H	L	H	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High transition of \overline{nLEXX} or \overline{nEXX} (XX = AB or BA)
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High transition of \overline{nLEXX} or \overline{nEXX} (XX = AB or BA)
X = Don't care
 \uparrow = Low-to-High transition of \overline{nLEXX} or \overline{nEXX} (XX = AB or BA)
NC= No change
Z = High impedance or "off" state

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LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		−0.5 to +7.0	V
I _{IK}	DC input diode current	V _I < 0	−18	mA
V _I	DC input voltage ³		−1.2 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	−50	mA
V _{OUT}	DC output voltage ³	output in Off or High state	−0.5 to +5.5	V
I _{OUT}	DC output current	output in Low state	128	mA
		output in High state	−64	mA
T _{stg}	Storage temperature range		−65 to 150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V _{CC}	DC supply voltage	4.5	5.5	V
V _I	Input voltage	0	V _{CC}	V
V _{IH}	High-level input voltage	2.0		V
V _{IL}	Low-level Input voltage		0.8	V
I _{OH}	High-level output current		−32	mA
I _{OL}	Low-level output current		64	mA
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T _{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T _{amb} = +25°C			T _{amb} = −40°C to +85°C		
				MIN	TYP	MAX	MIN	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 4.5V; I _{IK} = −18mA				−1.2		−1.2	V
V _{OH}	High-level output voltage	V _{CC} = 4.5V; I _{OH} = −3mA; V _I = V _{IL} or V _{IH}		2.5	3.0		2.5		V
		V _{CC} = 5.0V; I _{OH} = −3mA; V _I = V _{IL} or V _{IH}		3.0	3.6		3.0		V
		V _{CC} = 4.5V; I _{OH} = −32mA; V _I = V _{IL} or V _{IH}		2.0	2.7		2.0		V
V _{OL}	Low-level output voltage	V _{CC} = 4.5V; I _{OL} = 64mA; V _I = V _{IL} or V _{IH}			0.36	0.55		0.55	V
V _{RST}	Power-up output voltage ³	V _{CC} = 5.5V; I _O = 1mA; V _I = GND or V _{CC}			0.13	0.55		0.55	V
I _I	Input leakage current	V _{CC} = 5.5V; V _I = GND or 5.5V	Control pins		±0.01	±1.0		±1.0	μA
I _{HOLD}	Bus Hold current A or B Ports ⁵ 74ABTH161543	V _{CC} = 4.5V; V _I = 0.8V		35			35		μA
		V _{CC} = 4.5V; V _I = 2.0V		−75			−75		
		V _{CC} = 5.5V; V _I = 0 to 5.5V		±800					
I _{OFF}	Power-off leakage current	V _{CC} = 0.0V; V _O or V _I ≤ 4.5V			±1.0	±100		±100	μA
I _{PU/PD}	Power-up/down 3-State output current ⁴	V _{CC} = 2.1V; V _O = 0.0V or V _{CC} ; V _I = GND or V _{CC} ; V _{OE} = Don't care			±1.0	±50		±50	μA
I _{IH} + I _{OZH}	3-State output High current	V _{CC} = 5.5V; V _O = 5.5V; V _I = V _{IL} or V _{IH}			1.0	50		50	μA
I _{IL} + I _{OZL}	3-State output Low current	V _{CC} = 5.5V; V _O = 0.0V; V _I = V _{IL} or V _{IH}			−1.0	−50		−50	μA
I _{CEX}	Output High leakage current	V _{CC} = 5.5V; V _O = 5.5V; V _I = GND or V _{CC}			1.0	50		50	μA
I _O	Output current ¹	V _{CC} = 5.5V; V _O = 2.5V		−50	−100	−200	−50	−200	mA
I _{CCH}	Quiescent supply current	V _{CC} = 5.5V; Outputs High, V _I = GND or V _{CC}			0.50	1.5		1.5	mA
I _{CCL}		V _{CC} = 5.5V; Outputs Low, V _I = GND or V _{CC}			9	19		19	mA
I _{CCZ}		V _{CC} = 5.5V; Outputs 3-State; V _I = GND or V _{CC}			0.50	1.5		1.5	mA
ΔI _{CC}	Additional supply current per input pin ² 74ABT161543	V _{CC} = 5.5V; one input at 3.4V, other inputs at V _{CC} or GND			5.0	100		100	μA
ΔI _{CC}	Additional supply current per input pin ² 74ABTH161543	V _{CC} = 5.5V; one input at 3.4V, other inputs at V _{CC} or GND			0.20	1		1	mA

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100μsec is permitted.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

16-bit latched transceiver with dual enable and master reset (3-State)

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AC CHARACTERISTICS

GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V			T _{amb} = −40 to +85°C V _{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay nAx to nBx, nBx to nAx	2	1.2 1.0	2.5 2.2	3.4 2.9	1.2 1.0	3.9 3.5	ns
t _{PLH} t _{PHL}	Propagation delay LEBA to nAx, LEAB to nBx	1 2	1.2 1.2	3.0 2.6	4.1 3.5	1.2 1.2	5.1 4.1	ns
t _{PHL}	MRba to nAx, MRab to nBx	6	1.2	2.6	3.4	1.2	4.2	ns
t _{pZH} t _{pZL}	Output enable time OEBA to nAx, OEAB to nBx	4 5	1.4 1.4	3.3 3.4	4.4 4.4	1.4 1.4	5.5 5.6	ns
t _{PHZ} t _{PLZ}	Output disable time OEBA to nAx, OEAB to nBx	4 5	1.4 1.4	3.5 2.7	4.8 3.5	1.4 1.4	5.4 4.0	ns
t _{pZH} t _{pZL}	Output enable time EBA to nAx, EAB to nBx	4 5	1.4 1.4	3.4 3.5	4.4 4.4	1.4 1.4	5.6 5.7	ns
t _{PHZ} t _{PLZ}	Output disable time EBA to nAx, EAB to nBx	4 5	1.3 1.3	3.5 2.7	4.4 3.5	1.3 1.3	5.4 4.0	ns

AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

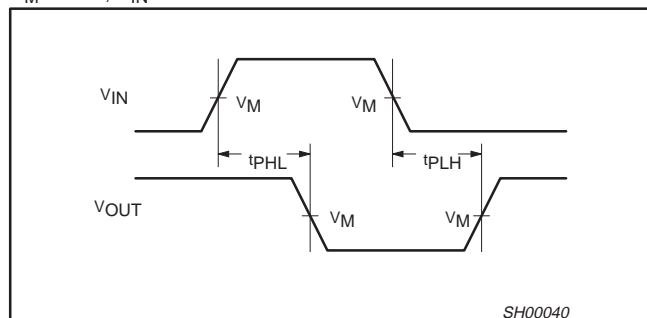
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$		$T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$	
			MIN	TYP	MIN	
$t_s(\text{H})$ $t_s(\text{L})$	Setup time nAx to $\overline{\text{LEAB}}$, nBx to $\overline{\text{LEBA}}$	3	1.5 2.0	-0.3 0.1	1.5 2.0	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time nAx to $\overline{\text{LEAB}}$, nBx to $\overline{\text{LEBA}}$	3	1.5 2.0	-0.1 0.1	1.5 2.0	ns
$t_s(\text{H})$ $t_s(\text{L})$	Setup time nAx to $\overline{\text{EAB}}$, nBx to $\overline{\text{EBA}}$	3	1.5 2.0	-0.1 0.2	1.5 2.0	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time nAx to $\overline{\text{EAB}}$, nBx to $\overline{\text{EBA}}$	3	1.5 2.0	-0.1 -0.1	1.5 2.0	ns
$t_w(\text{L})$	Latch enable pulse width, Low	3	4.0	2.0	4.0	ns
$t_w(\text{L})$	$\overline{\text{MR}}$ Pulse width, Low	6	3.0	1.0	3.0	ns

16-bit latched transceiver with dual enable and master reset (3-State)

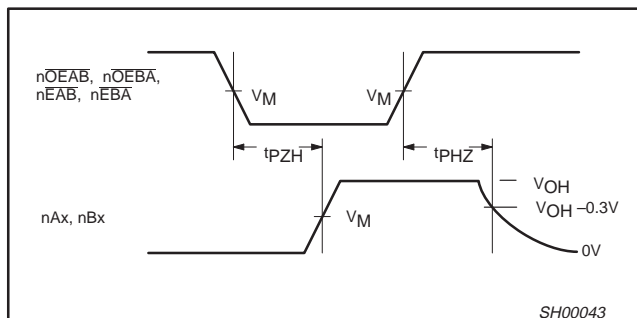
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AC WAVEFORMS

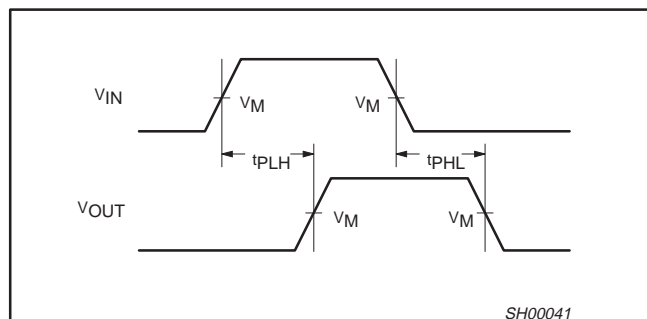
$V_M = 1.5V$, $V_{IN} = GND$ to $3.0V$



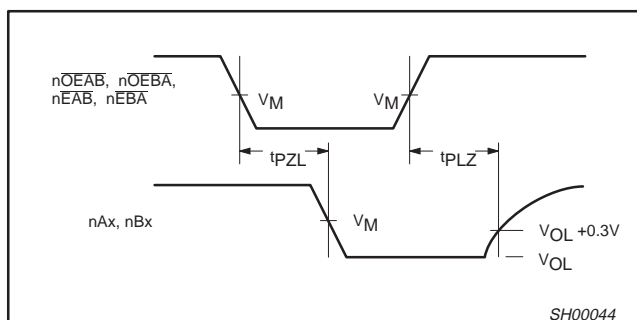
Waveform 1. Propagation Delay For Inverting Output



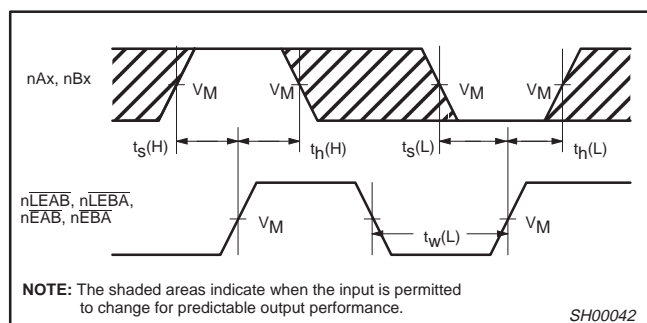
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



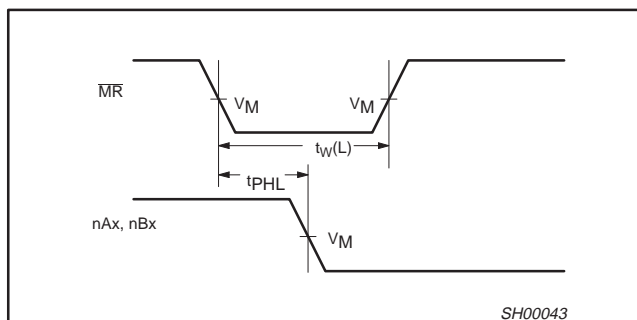
Waveform 2. Propagation Delay For Non-Inverting Output



Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level



Waveform 3. Data Setup and Hold Times and Latch Enable Pulse Width

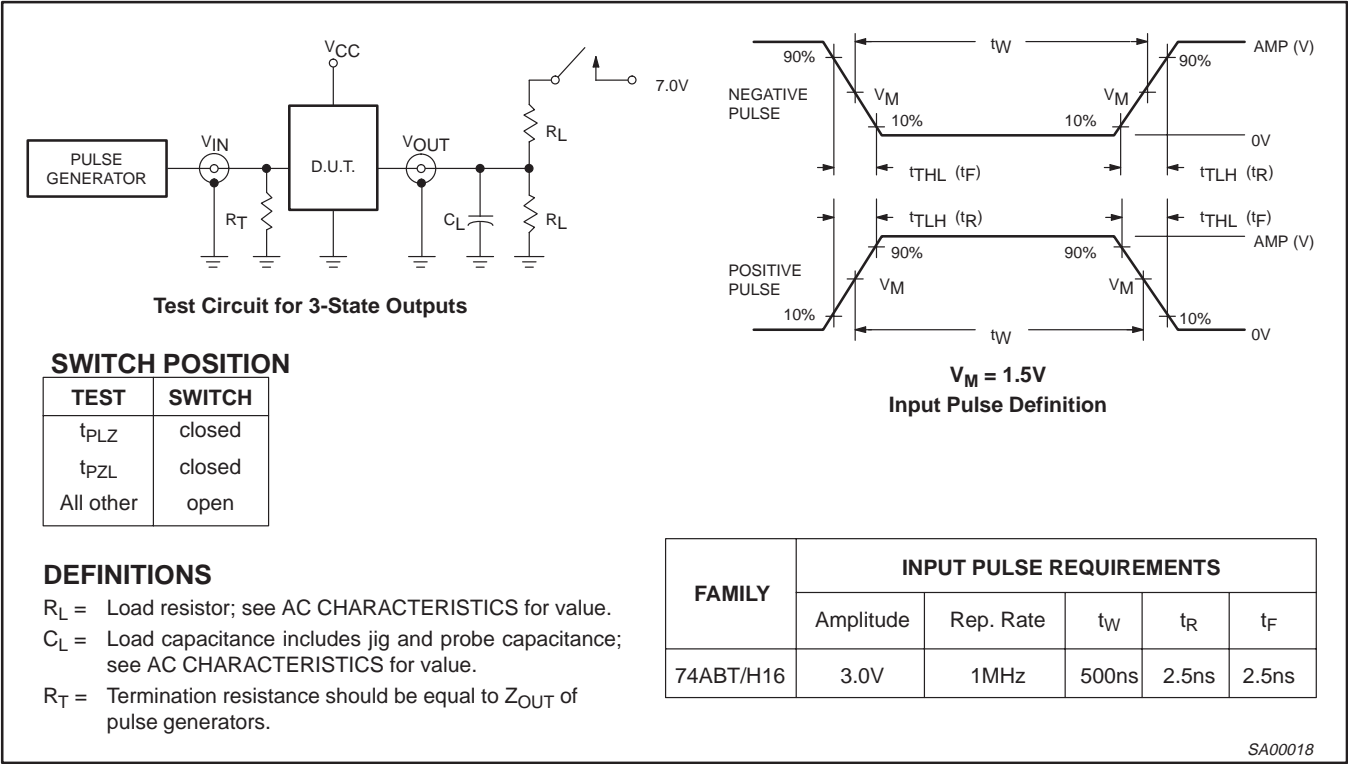


Waveform 6. Master Reset Pulse Width, Master Reset to Output Delay

16-bit latched transceiver with dual enable
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TEST CIRCUIT AND WAVEFORMS

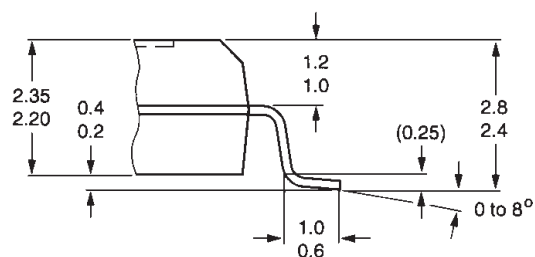
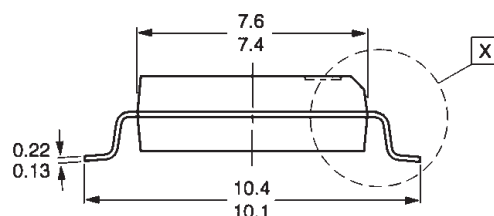
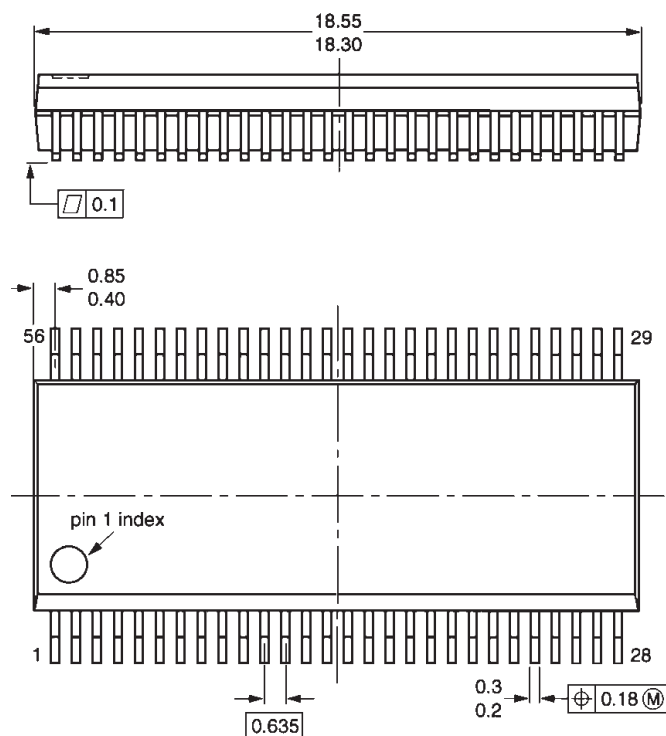


16-bit latched transceiver with dual enable and master reset (3-State)

74ABT161543
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SSOP56: plastic shrink small outline package; 56 leads; body width 7.5mm

SOT371-1



detail X

MSA406

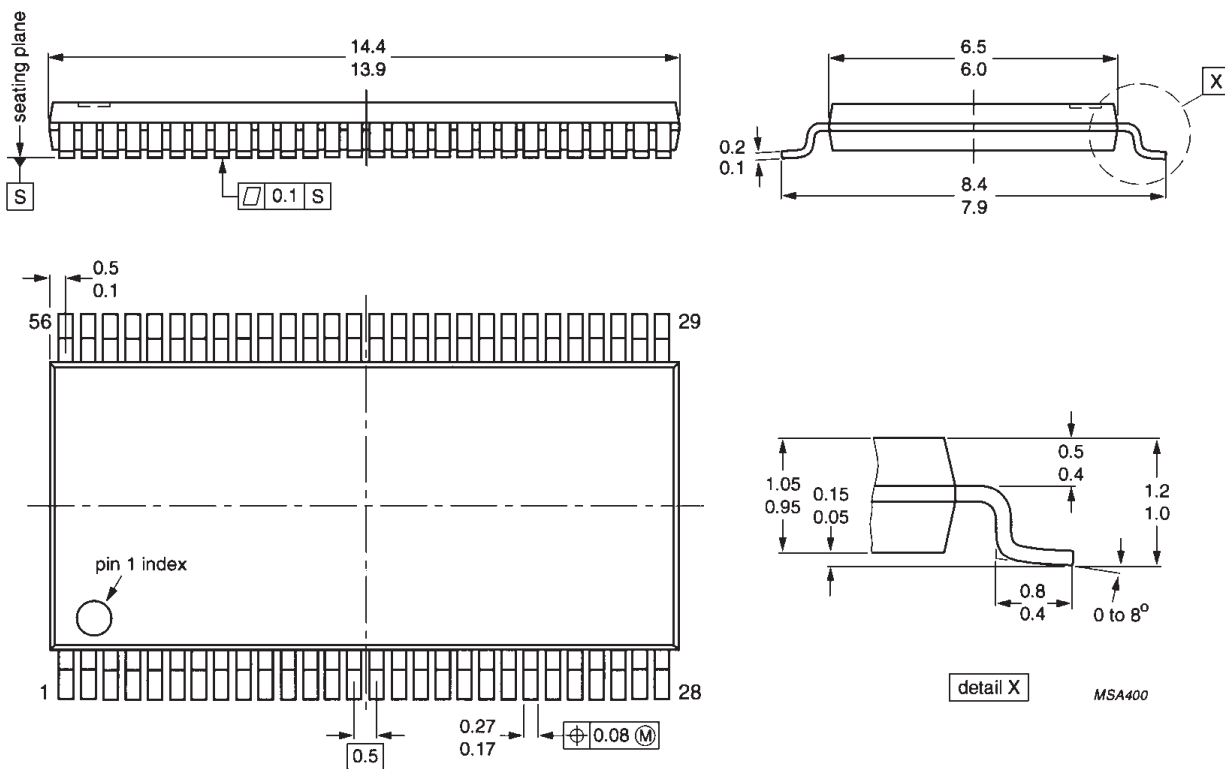
Dimensions in mm.

16-bit latched transceiver with dual enable and master reset (3-State)

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TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



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74ABTH161543

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088-3409
Telephone 800-234-7381

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